Valid from 2024.HS

Module description: Digital Technology Project

Module Code	t.BA.ET.PM2.19HS
ECTS Credits	4
Language of Instruction/Examination	German
Organizational Unit	InES
Module Coordinator	Matthias Rosenthal
Legal Framework	The module description is part of the legal basis in addition to the general academic regulations. It is binding. During the first week of the semester a written and communicated supplement can specify the module description in more detail.
Module Characteristic	Type 4* 4 lab lessons per semester week and half-class
Module Description	In this module a digital audio synthesizer is realized as a project on a programmable device (FPGA). Basic elements of digital technology such as combinatorial logic, digital counters and automats are applied playfully and creatively.
Module Content	• Theoretical knowledge in digital technology (DT), which was acquired in the last semester, is tested in practice in this project course. At the same time, the necessary skills for structuring as well as writing and giving oral presentations during project implementation will be developed. Project scope:· Conception, design, realization and testing of an audio synthesizer. The minimum features are DDS, Midi Decoder, Codec Controller, I2S Master; depending on the learning success, extra features can also be built in such as Melody Box, Play Recorder, LCD Display, FM Synthesis, Envelope.· Getting to know and installing various building blocks and their functional principles: Audio codec, I2C, I2S, DDS, Midi, FM synthesis· Plan VHDL Simulations and Design Test Benches· Document and present project results· Communicate in project teams
Prerequisite Knowledge	Besuch von Digitaltechnik (DT)

Learning Objectives (Competences)

Students...	Competencies	Taxonomies
Describing digital basic circuits (combinatorial logic, counters, shift registers, automats) in the programming language VHDL	F, M	K3
Manage a digital circuit from design phase to implementation on an FPGA prototype board	M, F	K5
Create high-quality project documentation	SE	K3
Being able to use a digital VHDL simulator	F, M	K3
To organise and participate in a project from its inception to its completion.	SE	K6
Successfully communicate internally and externally	SO	K5
Lead projects and their team members to the final goal, be able to perform constructive project meetings	SO	K6
Assess whether a project is achievable with given means in due time. Estimate project schedules, costs and personnel expenses.	SE	K6
Use tools to synthesize programmable logic and load custom logic descriptions onto CPLD/FPGA development boards	F, M	K3
Preparing and giving presentations	SE	K6

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Performance Assessment

End-of-module exam	Assessment	Length (min.)	Weighting	Form
oral exam			100	

Performance assessment during the semester	Assessment	Length (min.)	Weighting	Form
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Classroom Attendance Requirement	None
Learning material	
Comments	A project is realized during the lessons. The project will be accompanied by a communication lecturer.