Valid from 2024.HS

Module description: Computer Engineering 2

Module Code	t.BA.XX.CT2.10HS
ECTS Credits	4
Language of Instruction/Examination	German
Organizational Unit	InES
Module Coordinator	Andreas Rüst
Legal Framework	The module description is part of the legal basis in addition to the general academic regulations. It is binding. During the first week of the semester a written and communicated supplement can specify the module description in more detail.
Module Characteristic	Type 3a 2 lecture lessons per semester week and class+ 2 lab bi-weekly lessons per semester and half-class
Module Description	The module covers memory hierarchies and their implications for software. Students also learn the features and application of basic peripheral devices of microcontrollers. Specific emphasis is placed on software techniques for structuring embedded programs and controlling program flow.
Module Content	**The module covers the expansion of a processor to a complete computer system. On the one hand, this comprises memory hierarchies, cache and virtual memory including their implications on software. On the other hand, students learn the the features and application of basic peripheral devices of microcontrollers. Specific emphasis is placed on software techniques to structure embedded programs and to control program flow.** **From processor to system** • Organization of a microcontroller • Functionality of a system bus • Memory map and address decoding • Functionality and application of control- and status registers **Application of peripheral devices** • Connecting IOs through GPIO • Serial data transfer: UART / SPI / I2C • Timer / Counter and their applications • Analog Digital Converter (ADC) • Hardware Abstraction **Memory hierarchies** • Memory technologies: Volatile (SRAM, DRAM) vs. non-volatile (ROM, Flash, EEPROM) • Connecting external memory devices • Cache: Temporal and Spatial Locality, implications on software **Control flow in programs** • Structuring of a program into modules • Software State-Machines (State-Event Model) • Detection of events: Polling vs. interrupt-driven IO • Interrupt performance and latency **Hardware oriented programming labs for a target system** • Working with Cross-Compiler, Linker, Loader and Debugger
Prerequisite Knowledge	The module requires the material from Computer Engineering 1 (CT1)

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Learning Objectives (Competences)

Students...	Competencies	Taxonomies
After the course, students are able to understand the organization and the functionality of a microcontroller. They can interpret timing diagrams of a system bus, understand address decoding and are able to write programs that access control and status registers.	M, F	K2, K3
Students are familiar with basic concepts for sequential control of program flow. They can model and implement a task as a software state-machine. They can discuss methods to detect events and can analyze them with regard to performance and latency.	F, M	K2, K3, K4
Students are able to give an overview of the major types of memory. Moreover, they are able to connect external memory device and to explain a typical memory hierarchy. They can explain the functionality of caches and can assess the implications on software.	F, M	K2, K3
For microcontrollers, students can describe the features and functions of basic peripheral devices. Moreover, they can use such devices in their own programs - either directly or with a Hardware Abstraction Layer. In addition, students can access external peripheral devices through serial communication (UART, SPI, I2C).	M, F	K2, K3

Performance Assessment

End-of-module exam	Assessment	Length (min.)	Weighting	Form
written exam	Grade	90	70	acc. to module agreement

Performance assessment during the semester	Assessment	Length (min.)	Weighting	Form
written exam	Grade	45	15	acc. to module agreement
Labs with presentations	Grade		15	acc. to module agreement

Classroom Attendance Requirement

None

The labs have to be submitted on site during the lab lessons.

Learning material

- Data Sheets and User Manual
- Exercises
- Lab descriptions
- Slides

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Comments	**Mandatory mid-term exam:** Date according to course schedule. Missed exams: Dispensation in advance possible for justified cases. Afterwards only with medical certificate. Resit can be an oral exam. Missed exams without dispensation will receive a 1.0 grade. **Labs:** grading based on the presence and number of solved labs. Lab solutions (programs) have to be presented and explained to the lecturer. **Semester end exam:** Written exam or moodle, open book, without generative AI. Covers the topics from lectures and labs.